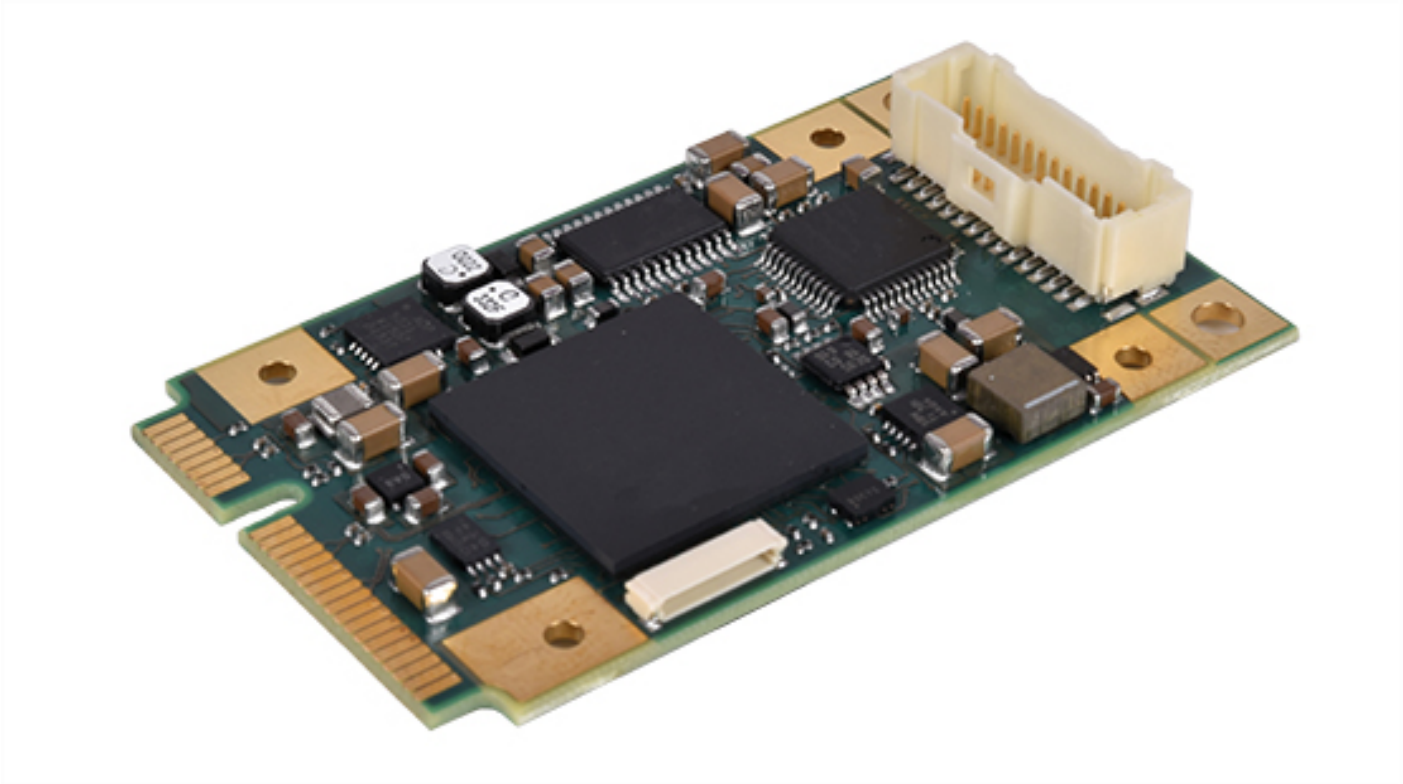
IO397

FPGA I/O Module

Hardware Reference Manual



v1.2

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Contents

1 Document Version History

Version	Chapter	Changes	Author	Date
1.0	–	Initial release	SiBe	21 Nov. 2022
1.1	4.1.2, 4.1.3	Textual changes	DaHa	04 Oct. 2023
1.2	6.2.2	Added terminal board SH pin to mapping table	BeSc	09 Feb 2024

2 Technical Information

Description

The IO397 I/O module is a mPCIe- compatible, Simulink-programmable FPGA and configurable FPGA I/O module combining accurate analog and digital input and output channels with a large selection of standard interfaces such as PWM, SPI, and I2C. This I/O module is ideal for closed-loop controls and hardware-in-the-loop (HIL) simulations using MATLAB® and Simulink.

In addition, take advantage of Speedgoat's HDL I/O Blocksets for the Simulink-programmable FPGA workflow to achieve high-demanding closed-loop applications where sample rates are greater than 20 kHz. Alternatively, you can choose Speedgoat's configurable workflow for applications with closed-loop sample rates less than 20 kHz.

Features

- 14 ESD-protected TTL I/O lines with pull-resistors. Voltage levels of +3.3 V, +5 V, or ground, and input/output directions that are software configurable by I/O line
- 4x 16-bit analog inputs, 200 kSPS, ADC
- 4x 16-bit analog outputs with a 10 µs settling time
- Configurable workflow for Simulink Real-Time™ supported by Speedgoat configuration files and the Speedgoat I/O Blockset
- Simulink-programmable FPGA workflow to use HDL Coder™ and Simulink Real-Time™ supported by the Speedgoat HDL Coder Integration Package

3 Technical Specifications

Physical		
Form factor	mPCIe	
Power requirements	+3.3 Vaux: 650 mA typical	
Bus	PCI Express	
Connectors	Digital: 17-pin M12 male Cable connector: Phoenix Contact M12 17-pos female connector Board connector: Phoenix Contact part no. 1442078	Analog: 17-pin M12 female Cable connector: Phoenix Contact M12 17-pos male connector Board connector: Phoenix Contact part no. 1442081
Environmental		
Operating temperature	-40 °C to +85 °C	
Relative humidity	5 to 95 %, non-condensing	
Analog Input		
Number of inputs	4	
ADC resolution	16	
Max ADC sample rate	200 kSPS	
Input Filter	1st order, 100 kHz -3 dB cutoff frequency	
Voltage ranges	Software-selectable 0-5.12 V, 0-10 V, 0-10.24 V, ±5 V, ±5.12 V, ±10 V and ±10.24 V	
Analog Output		
Number of outputs	4	
DAC resolution	16	
Settling time (2kΩ/4000 pF)	<10 µs	
Update rate	Configurable workflow: 50 kHz Programmable FPGA workflow : $\frac{1}{4*(\frac{(floor(\frac{F_{FPGA}}{30e^6})+1)}{F_{FPGA}})*24+(\frac{floor(200e^{-9}*F_{FPGA})}{F_{FPGA}})}$ e.g., ca. 213.7 kHz @ F_{FPGA} = 100 MHz	
Voltage range	0-5 V, 0-10 V, ±5 V, ±10 V	
Output current	10 mA	
FPGA		
FPGA chip	Xilinx Artix-7 XC7A50T	
Speedgoat product name	IO397	
No. of logic cells available	50k	
Digital I/O		
TTL	14 ESD-protected TTL I/O lines with pull-resistors. Voltage levels of +3.3 V, +5 V, or ground, and input/output directions that are software configurable by I/O line	
Reliability		
Mean time between failures (MTBF)*	987,000 hours	

4 Handling and Operating Instructions

4.1 ESD Protection

The module is sensitive to static electricity. Appropriate care must be taken when packing, unpacking and handling the module.

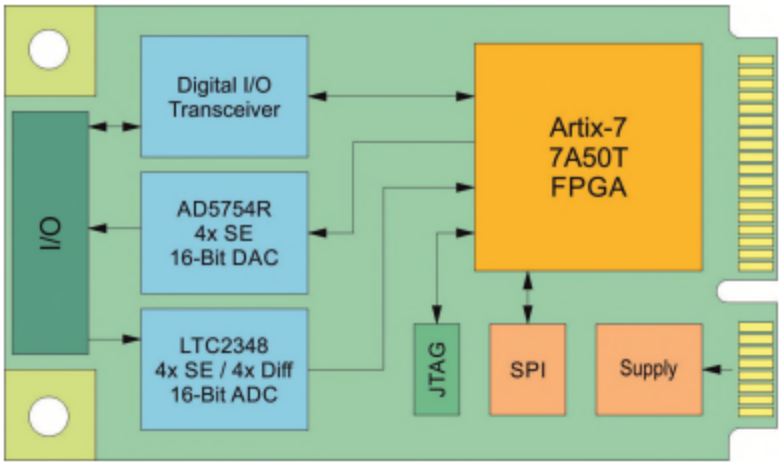
4.2 I/O Interface Installation

Signals are available on both the front and rear connectors.
Only one connector can be used/installed at a time.

4.3 Assembly Recommendations

When removing the module from the carrier board, ensure mechanical stress is kept as low as possible.

5 Functional Description



IO397 I/O module block diagram

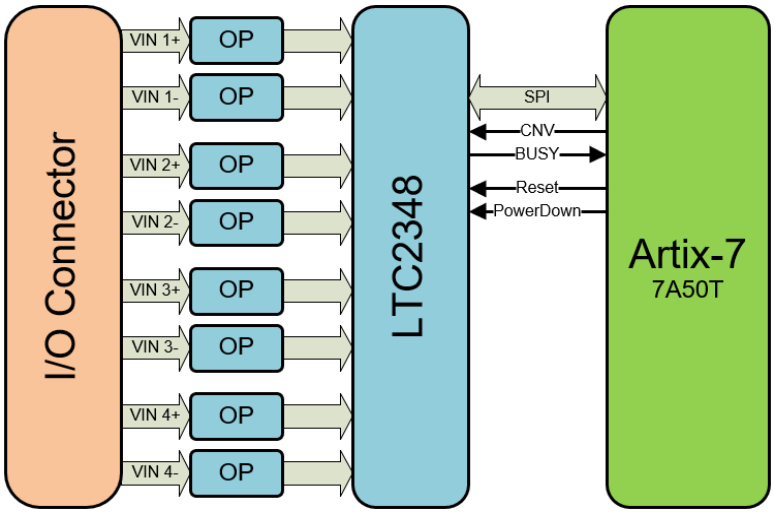
5.1 Analog Input

5.1.1 Overview

The 4 analog inputs of the IO397 are implemented with a LTC2348-16 ADC device. This SAR-ADC has an eight-channel differential input MUX: only 4 of these channels are used with an integrated Programmable Gain Amplifier (PGA).

The LTC2348-16 ADC provides a Serial Peripheral Interface (SPI) for the digital connection to the user FPGA. In addition, four additional control lines (RESET, Power-Down, Busy and CNV) for general and conversion process control are available.

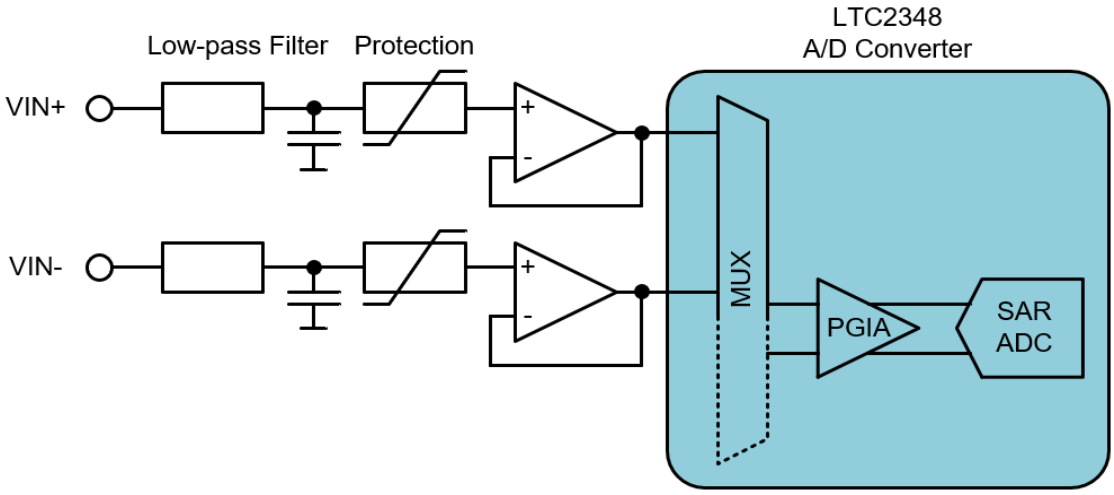
The ADC is connected via a dedicated SPI bus, a conversion control line CNV and a BUSY status line to the user FPGA.



ADC Input Structure

5.1.2 Input Stage

The IO397 Analog Input Stage provides:



Analog Input Stage

Input Filter

The IO397 features a 1st order low-pass filter at the analog inputs for suppressing noise on the analog input lines (for example, coupled noise from switching digital I/O lines running in the same I/O cable) and to avoid sampling errors related to Nyquist theorem. The -3 dB cutoff frequency of the input filter is approximately 100 kHz.

Input Protection

The absolute input voltage limit for the analog inputs is ±11 V relative to ground for each pin. The common mode range is limited by the buffer amplifier.

Input Buffer

The IO397 provides analog input operation amplifier buffers for decoupling the analog signal source.

ADC Device Internal Input Path

The LTC2348-16 is an ADC with multiplexed analog inputs. Inside the LTC2348-16 chip, the analog input channels (pins) are connected to a single internal gain amplifier and a single internal SAR ADC unit by way of an internal analog multiplexer. However, the LTC2348-16 samples all analog inputs at the same point of time with the CNV command. The conversion of the digital values of all channels are processed sequentially; therefore, all channels are sampled at the same time and the conversion time is always the same no matter how many channels are used.

Protection	4 kV ESD HMB rating on analog input channels ±55 V power-off and overvoltage protection
Input Impedance	>1 GΩ
Input Capacitance	5 pF
Common-Mode Input Range	±11 V

ADC Electrical Interface

5.1.3 Sample Rate

The 4 analog inputs of the IO397 I/O module are implemented with one 8-channel ADC device (whereby only 4 channels are used) with simultaneous sampling and parallel data transmission; therefore, the conversion time remains the same no matter how many channels are used. The maximum sample rate is 200 kSPS.

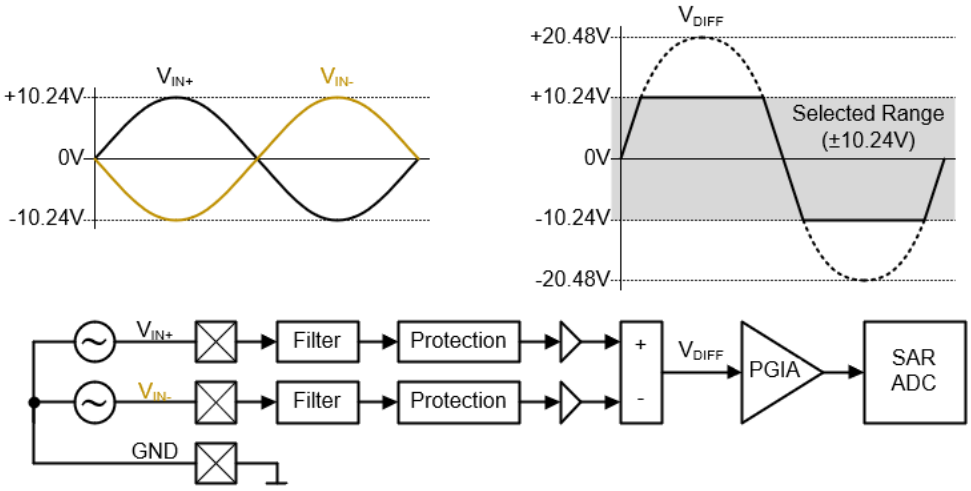
5.1.4 Voltage Range

An LTC2348 integrated PGIA (programmable gain instrumentation amplifier) is used to adapt the analog input voltage range to the internal (fix) SAR ADC voltage range.

5.1.4.1 Differential Measurement

The LTC2348 ADC device always measures differential signals.

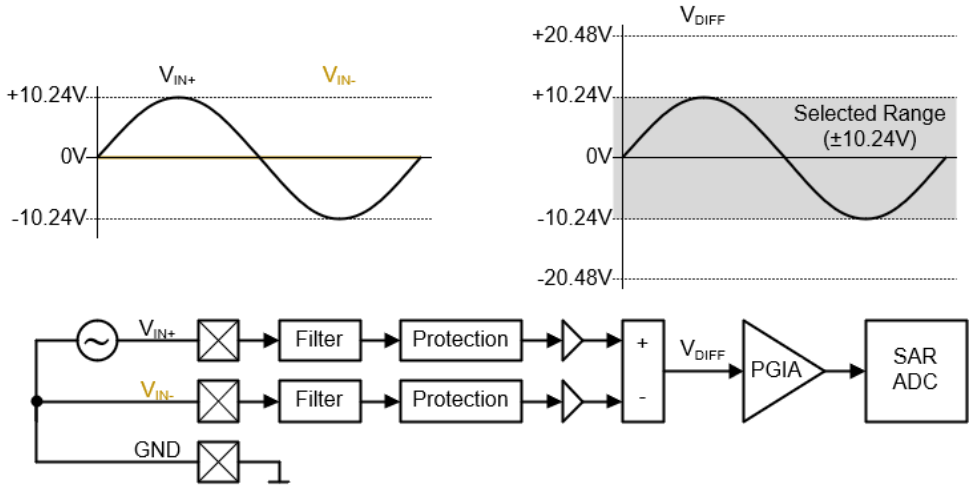
The differential measurement contains a positive (+) and a negative (-) input signal. The maximum operating range for the analog inputs is ±10.24 V (to GND). The range of possible differential measurements therefore is ±20.48 V. The ADC measurement can be set to different ranges. Depending on the configured range, the corresponding differential measurement is limited. The following example shows the details with the ADC range set to ±10.24 V:



Differential Measurement: The signal to measure can reach double the range of each single input.

5.1.4.2 Single-Ended Measurement

For single-ended measurements, only the (+) input is used. The (-) input in this case must be connected to GND. The range of single-ended measurements is therefore limited to ±10.24 V as depicted in the following figure:



Single-ended measurement: The signal to measure can only reach the range of the channel input

5.1.4.3 Available Ranges

The following table provides an overview of the analog input ranges supported.

ADC Channel Configuration Option		Differential Mode Analog Input Range [2]		Single-Ended Mode Analog Input Range
Voltage Range	LSB	V_{IN+} Range to GND V_{IN-} Range to GND	V_{IN_DIFF} Range $V_{IN\_DIFF} = V_{IN+} - V_{IN-}$	V_{IN} Range to GND
±10.24 V	312.5 µV	±10.24 V	±10.24 V	±10.24 V
±10.0 V	305.18 µV	±10.24 V	±10.0 V	±10.0 V
±5.12 V	156.25 µV	±10.24 V	±5.12 V	±5.12 V
±5.0 V	152.59 µV	±10.24 V	±5.0 V	±5.0 V
0.0 V to 10.24 V	156.25 µV	±10.24 V	±2.56 V	±2.56 V
0.0 V to 10.0 V	152.59 µV	±10.24 V	±1.28 V	±1.28 V
0.0 V to 5.12 V	78.125 µV	±10.24 V	±0.64 V	±0.64 V

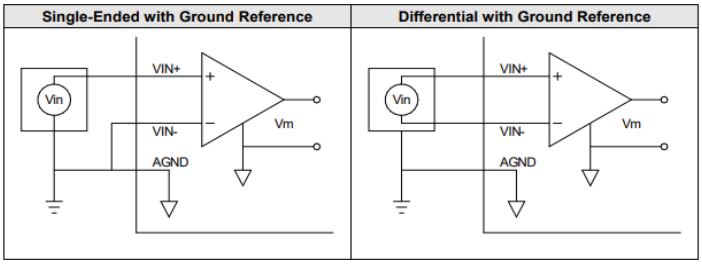
Analog Input Ranges

[1] ± Indicates a voltage range (for example, ±5.12 V is used as a short form for -5.12 V … +5.12 V)
[2] The V_{IN+} and V_{IN-} voltage levels must comply with both given ranges (range when referenced to ground and differential voltage range). For example, when the ADC voltage range is set to ±5.12 V and V_{IN+}= 10.0 V (to ground) and V_{IN-} =8.0 V (to ground), the resulting voltage is 10.0 V - 8.0 V = 2.0 V which is within the range of ±5.12 V

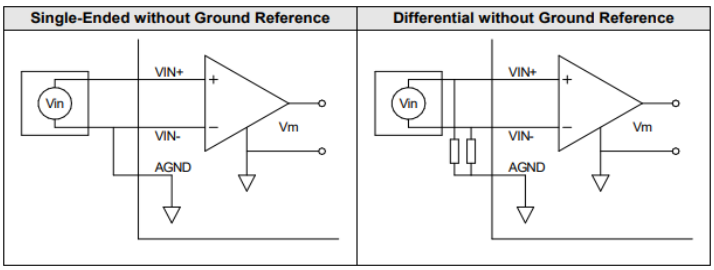
The ranges were calibrated as part of the factory tests. The correction values determined were stored in an I2C EEPROM and are automatically applied within the Speedgoat integration of the IO397 I/O module.

Due to the tolerances of the reference voltage generation, the basic tolerances of the ADC components, and the temperature dependency, it may be that the limits for the input voltage cannot be achieved.

5.1.5 Front I/O - Analog Input Connections



If signals without a ground reference need to be connected, connect VIN+ and VIN- to GND with a resistor to prevent the signal source from floating out of the ADC's common-mode range. In most cases, a weak resistor to ground at the VIN- connection suffices:



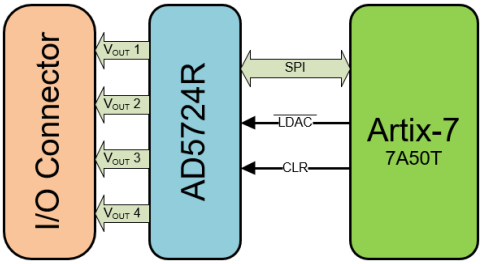
5.2 Analog Output

5.2.1 Overview

The 4 analog DAC outputs of the IO397 are implemented with one AD5754R 16-bit DAC device.

The interface to the DAC is realized with an SPI interface and separate signals to load all DAC outputs. All the DAC channels are therefore loaded sequentially and the conversion of all channels is then started simultaneously.

The following figure shows the structure and principle of the DAC outputs :



Analog Output Selection

5.2.2 Update Rate

The four analog outputs of the IO397 I/O module are implemented with one 4-channel DAC device with serial conversion. All channels of the DAC device are processed in a sequence. The interface always transfers all channels, therefore the update rate is always the same, no matter how many DAC channels are used.

Configurable Workflow

When using the configurable workflow, the DAC Update rate is fixed to 50 kHz.

Programmable Workflow

When using the programmable workflow, the Frequency of the FPGA F_{FPGA} can be defined by the user. In this case the DAC update rate is:

$$\frac{1}{4*\left(\frac{(floor(\frac{F_{FPGA}}{30e^6})+1)}{F_{FPGA}}\right)*24+\left(\frac{floor(200e^{-9}*F_{FPGA})}{F_{FPGA}}\right)}$$

e.g., ca. 213.7 kHz @ F_{FPGA} = 100 MHz

5.2.3 Voltage Range

The output voltage ranges of the IO397 DAC outputs are defined using the Simulink driver blocks, which in turn set the corresponding registers of the AD5754R device.

The following output voltage ranges are available: 0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V.

The ranges were calibrated as part of the factory tests. The correction values determined were stored in an I2C EEPROM and are automatically applied within the Speedgoat integration of the IO397 I/O module.

Due to the tolerances of the reference voltage generation, the basic tolerances of the DAC components, and the temperature dependency, it may be that the limits for the output voltage cannot be achieved.

5.2.4 Front I/O - Analog Output Connection

All analog outputs of the AD5754R DAC are directly routed through operational amplifiers to the front I/O connector.

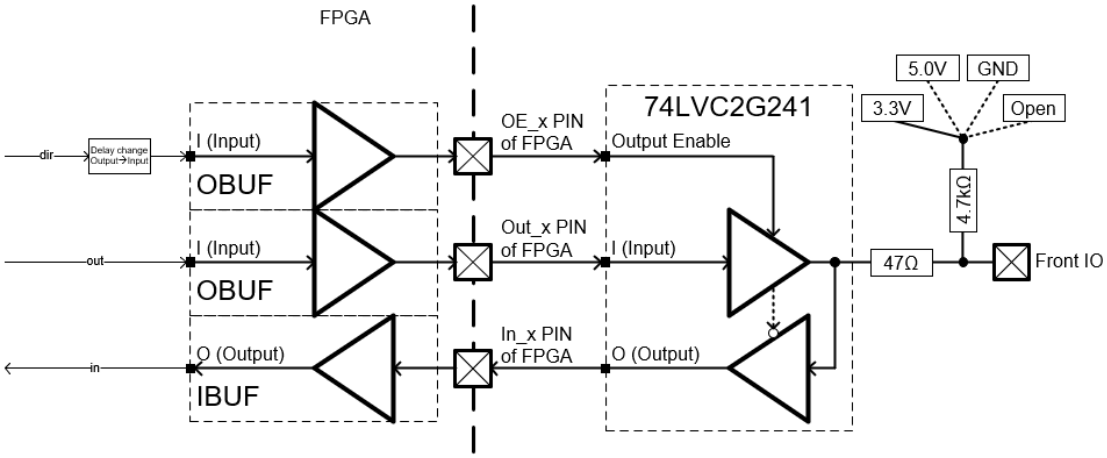
Protection	3.5 kV ESD HMB rating on analog input channels
Maximum Resistive Load	2000Ω
Maximum Capacitive Load	4000 pF
DC Output Impedance	

DAC Electrical Interface

5.3 Digital I/O

5.3.1 TTL I/O Interface

Each of the 14 front I/O TTL lines are designed with a 74LVC2G241 dual buffer as an interface to the user-FPGA (Artix-7) pins. The logic levels of the buffers are TTL compatible, meaning that the minimum high level is 2.0 V and the maximum low level is 0.8 V. The nominal output high voltage is 3.3 V. The following image depicts a single TTL line in detail:



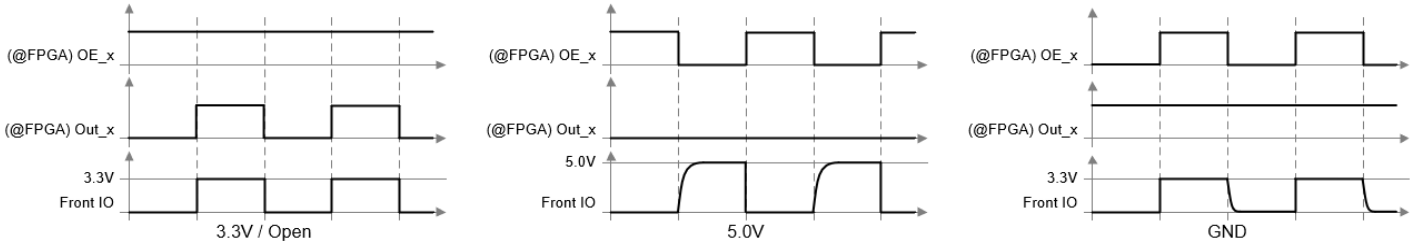
TTL Line Detail

The buffer outputs are followed by 47Ω serial resistors for signal integrity and safety reasons, as well as 4.7kΩ pull resistors.

There are several options for these pull resistors:

- 3.3 V pull-up: TTL line is pulled up to 3.3 V. For outputs, LOW and HIGH level are hard driven
- 5.0 V pull-up: TTL line is pulled up to 5.0 V. For outputs, LOW level is hard driven, and HIGH level is weakly driven
- GND pull-down: TLL line is pulled down to GND. For outputs, LOW level is weakly driven, and HIGH level is hard driven
- Float: TTL line is floating. For outputs, LOW and HIGH levels are hard driven (0 V / 3.3 V)

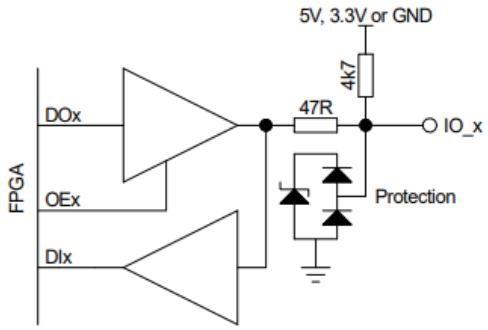
The following image depicts the different pull-settings if a TTL line is acting as an output. Weak driving of the signal means that the corresponding output enable signal of a TTL line is not active:



TTL output details with different pull-settings

The 5.0 V pull-up and the GND pull-down resistor can therefore only drive high impedance inputs. In low impedance input cases there is a reduced high-level voltage at the I/O pin when the output buffer sources a noticeable current to the external load while driving a high-level. There is also an increased low-level voltage at the I/O pin when the output buffer sinks a noticeable current from the external load while driving a low-level. The maximum current must be limited in both cases to ensure the signal level is correct.

A TVS array protects against ESD shocks:



TTL output detail with ESD protection

Due to placement restrictions, groups are required for the pull voltage. All 14 TTL lines are grouped.

If the Pull-Resistor is set to float (possible selection), the user should bear in mind that all I/O lines are connected via their Pull-Resistors.

5.4 Board Management

5.4.1 Xilinx Artix-7 FPGA

The FPGA on the IO397 I/O module is a Xilinx Artix-7 XC7A50T-2CSG325I. The Xilinx Artix-7 is supported by the Xilinx Vivado ML Standard Edition.

At power-up, the FPGA of the IO397 I/O module is always configured via the SPI Flash memory with the last used bitstream configuration. During deployment of the Simulink real-time application, the customer-created FPGA bitstream is loaded onto the onboard SPI Flash if it differs from the FPGA bitstream configured using the PCIe interface. After the FPGA bitstream download, the FPGA is re-loaded with the newly updated bitstream on the SPI flash and the application can start.

5.4.2 PCIe Interface Logic

The PCIe bus interface logic implemented in the IO397 I/O module design provides a PCIe interface to the carrier with 1 lane.

The PCIe bus endpoint interface logic is contained within the FPGA. This logic includes support for PCIe commands, such as configuration read/write, and memory read/write.

5.4.3 Clock Generation

There is one FPGA reference clock source available for user logic.

The PCI Express Mini Card Slot provides a 100 MHz clock to the D5/D6 FPGA global clock input pin. The IO397 design uses the 62.5 PCIE-AXI clock to generate the user FPGA Clock by inserting a MMCM.

Configurable Workflow

When using the configurable workflow, the user FPGA clock is fixed to 75 MHz (derived from the 62.5MHz PCIE-AXI clock).

Programmable Workflow

When using the programmable workflow, the user FPGA clock can be defined by the user. Note that it is derived from the 62.5MHz PCIE-AXI clock with an MMCM. This means that the possible FPGA clock settings are limited to the capabilities of the MMCM on the Artix-7 FPGA device.

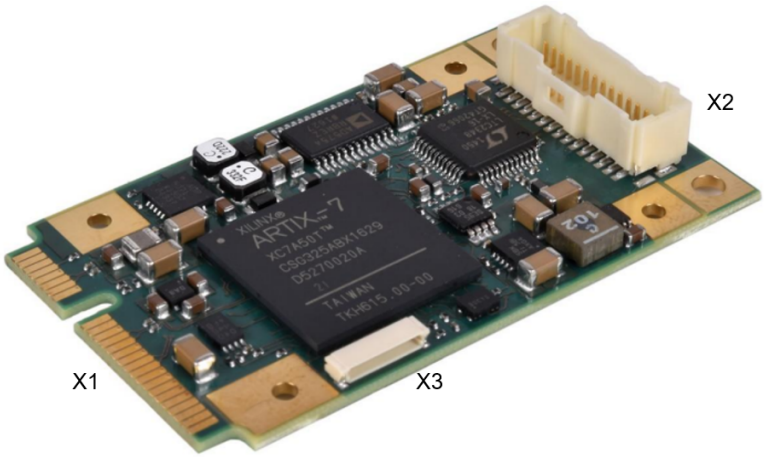
5.4.4 SPI Flash Memory

The FPGA is configured by a serial SPI flash during power-up. The SPI flash device (a Micron N25Q128A 128-Mbit serial flash memory), is in-system programmable (the Vivado device "mt25ql128" is used). A factory default configuration bitstream is stored in this flash memory. As mentioned earlier, the flash is overwritten by a customer FPGA configuration bitstream as soon as a model is deployed.

5.4.5 Power System Device

A PCI Express Mini Card slot is powered by two supplies: 1.5 V and 3.3 Vaux. While the 1.5 V is powered on and off with the rest of the system, the 3.3 Vaux supply is typically powered by the system's auxiliary power, which is available even when the system is off. Keep this in mind when installing or removing a PCI Express Mini Card and make sure that the system is turned off completely. After initial power-up, the FPGA on the IO397 is not configured until all power supplies are available. However, when the system is turned off, the FPGA remains configured as long as the slot is powered with the system's auxiliary power. In this case, a “power cycle” may not have the expected results.

6 I/O Connector



I/O Connector overview

6.1 System Connector (X1)

Pin count	52
Connector type	Card-edge
Source & Order Info	none

6.2 Front I/O Connector (X2)

Pin count	30
Connector type	Molex Pico-Clasp, dual row straight header, with lock
Source & Order Info	501190-3017
Mating cable connector	501189-2010

6.2.1 Front I/O Connector (X2) Pin Mapping

The I/O connector comes pre-connected to the front I/O of your real-time target machine. For the pinout of the M-12 front connectors for specific custom implementations, please refer to the documentation supplied with your configuration file or the HDL Coder Integration Package.

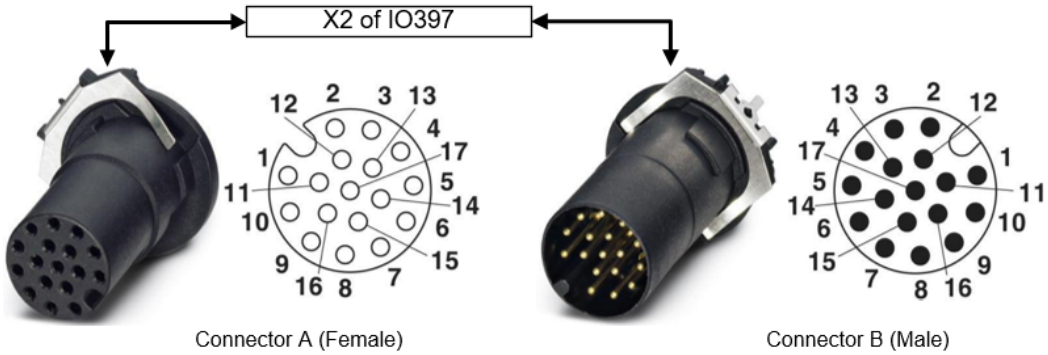
The I/O pin assignments below are for reference.

Pin	Single-Ended	Differential	Pin	Single-Ended	Differential
1	ADC 1	ADC 1+	2	Connect to GND	ADC 1-
3	ADC 2	ADC 2+	4	Connect to GND	ADC 2-
5	ADC 3	ADC 3+	6	Connect to GND	ADC 3-
7	ADC 4	ADC 4+	8	Connect to GND	ADC 4-
9	DAC 1	-	10	DAC 2	-
11	DAC 3	-	12	DAC 4	-
13	GND	GND	14	GND	GND
15	I/O_0	-	16	I/O_1	-
17	I/O_2	-	18	I/O_3	-
19	I/O_4	-	20	I/O_5	-
21	I/O_6	-	22	I/O_7	-
23	I/O_8	-	24	I/O_9	-
25	I/O_10	-	26	I/O_11	-
27	I/O_12	-	28	I/O_13	-
29	GND	GND	30	GND	GND
-	+5V	+5V	-	0V	0V

6.2.2 Front I/O (X2) Connector to Phoenix M12

As mentioned above, the front I/O comes pre-connected to two Phoenix M12 connectors. Two connectors are available (A, female and B, male).

Pin count	17
Connector type	Phoenix Contact M12
Source & Order Info (A female)	Phoenix Contact part no. 1442078
Source & Order Info (B male)	Phoenix Contact part no. 1442081
Mating cable connector	The two connectors below are mating connectors: - 17-pin M12 Male, Conn A (Phoenix Contact part no. 1424196) - 17-pin M12 Female Conn B (Phoenix Contact part no. 1424197)



IO397 X2 to Molex12 connections

Molex-Pin	Single-Ended	Differential	Molex-Pin	Single-Ended	Differential
A1	ADC 1	ADC 1+	A2	Connect to GND	ADC 1-
A3	ADC 2	ADC 2+	A4	Connect to GND	ADC 2-
A5	ADC 3	ADC 3+	A6	Connect to GND	ADC 3-
A7	ADC 4	ADC 4+	A8	Connect to GND	ADC 4-
A9	DAC 1	-	A10	DAC 2	-
A11	DAC 3	-	A12	DAC 4	-
A13	GND	GND	A14	GND	GND
A15	0V	0V	A16	5V DC	5V DC
A17	GND	GND	SH	Shielding of M12 cable	
B1	0V	0V	B2	5V DC	5V DC
B3	I/O_0	-	B4	I/O_1	-
B5	I/O_2	-	B6	I/O_3	-
B7	I/O_4	-	B8	I/O_5	-
B9	I/O_6	-	B10	I/O_7	-
B11	I/O_8	-	B12	I/O_9	-
B13	I/O_10	-	B14	I/O_11	-
B15	I/O_12	-	B15	I/O_13	-
B17	GND	GND	SH	Shielding of M12 cable	

6.3 JTAG Connector (X3)

Pin Count	10
Connector Type	JST XRS 10pol 0,6 mm Pitch IDC Connector
Source & Order Info	SM10B-XSRS-ETB
Mating Part	10XSR-36S

6.3.1 JTAG Connector (X3) Pin Mapping

Pin	Signal	Remarks
1	GND	
2	TCK	
3	TMS	
4	TDI	
5	TDO	
6	GND	
7	FPGA DONE	Also connected to GPIO0
8	Power Good	Also connected to GPIO1
9	PRESENT#	Not used by the IO397
10	V_{REF}	3.3 V level expected

7 Legal

As used herein, the term "Seller" shall mean Speedgoat GmbH, and term "Buyer" shall mean the person, firm or corporation executing a purchase order for "goods", sold by Seller (hereinafter "Products").

7.1 Limited Warranty

Seller warrants that the Products delivered hereunder shall be free from defects in workmanship and material under normal use and wear in accordance with Seller's instructions and specifications for a period of twenty-four (24) months from date of delivery to the Buyer, including component parts of Products sold as spare, replacement, maintenance or storage parts, which are also warranted for twenty-four (24) months from date of delivery, provided, however, in either case, that notice of any such defect is provided to Seller within thirty (30) days of its discovery by the Buyer. THE WARRANTY SET FORTH IN THIS SECTION SHALL BE IN LIEU OF ALL OTHER WARRANTIES, AND ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO WARRANTY OF MERCHANTABILITY, FITNESS FOR PARTICULAR PURPOSE, AND FITNESS FOR ORDINARY PURPOSE USED OR PURPOSE INTENDED, ARE EXCLUDED. IN NO EVENT SHALL SELLER, ITS EMPLOYEES OR SUPPLIERS BE LIABLE, EITHER DIRECTLY OR BY WAY OF INDEMNIFICATION, TO BUYER OR ANY THIRD PARTY FOR (A) AN AMOUNT EXCEEDING THE PURCHASE PRICE OF THE PRODUCT IN QUESTION AND (B) ANY PUNITIVE, EXEMPLARY, SPECIAL, INDIRECT OR CONSEQUENTIAL LOSSES, DAMAGES OR INJURIES regardless of whether such claim is based upon delays in delivery or payment, breach of warranty, breach of contract, strict liability, negligence, or any theory now known or hereinafter adopted by legislation or by any court. Neither Seller nor its affiliates shall be liable for any damage or loss to exposure of Products and/or their packaging to the elements (including but not limited to rain, snow, sleet, sun, wind, floods, etc.); chemicals, corrosive solvents or soils; unauthorized or improper use, maintenance, storage or repair; due to any failure to follow Seller's manuals, warnings, notices or instructions; or due to any malfeasance, recklessness or negligence by Buyer, any employee or costumer of Buyer or any other third party.

EXCLUSIVE REMEDY: In any event, the Buyer's exclusive remedy hereunder is limited to the furnishing of replacement parts on an exchange basis, or, at the option of Seller, to the repair or replacement of defective Products or replacement parts at one of Seller's locations, but in either case only if the defective Product or part has been submitted to Seller during the period of warranty. The Buyer accepts and acknowledges that the foregoing allocation of risk is reflected in the purchase price.

The parties further agree that if any portion of the foregoing exclusion of damages is held to be voidable or void by reason of public policy or unenforceable for any other reason whatsoever, all remaining portions of the foregoing exclusion shall continue in effect.

THE WARRANTY SET FORTH ABOVE DOES NOT EXTEND TO: Any systems that have been damaged or rendered defective as a result of accident, misuse, or abuse; by the use of parts not manufactured, authorized or sold by Seller; by modification or as a result of service by anyone other than Seller; systems not containing original components or original replacement of components; damage during shipment, unless due to incorrect packaging by Seller; systems that fail or are damaged after delivery due to shipment, handling, storage, operation, use or maintenance in manner or environment not conforming to any published instructions or specifications issued by Seller.

In-warranty repaired or replacement parts or Products are covered by warranty only for the remaining unexpired portion of the original warranty period applicable to the repaired or replaced parts or Products. In other words, repair or replacement of Products or parts under warranty does not extend the original warranty period.

Products that are no longer part of the regular sales offering are considered EOL (end-of-life) and are repaired on a best-effort basis.

EXTENDED HARDWARE WARRANTY SERVICE

Extended Hardware Warranty Service is available as an option and must be purchased at the time the Products are purchased for which the warranty shall be extended.

The Level One Hardware Warranty Service extends the standard 24-month warranty period by 12 months resulting in a 36-month warranty period.

The Level Two Hardware Warranty Service extends the standard 24-month warranty period by 36 months resulting in a 60-month warranty period.

Hardware warranty terms exceeding the 60-month range are available on request.

7.2 Returns

Buyer shall not return any Product without Seller's prior written consent. An RMA (Return Material Authorization) number issued by Seller must accompany all returned material. An RMA number can be obtained by contacting the Seller's support department (support@speedgoat.com).

Within Warranty, Products returned and needing corrective repair are serviced at no-charge in accordance with the terms of Seller's Warranty policy.

Repairs on out of Warranty Products are performed at Buyer's expense.

Please pack the returned Products in their original shipping cartons, or in equivalent strong protective shipping cartons. Shipping costs from Buyer to Seller associated with warranty repairs or replacements shall be borne by the Buyer. Shipping costs for the return of repaired goods from Seller to Buyer shall be borne by Seller.

7.3 Systems Software Maintenance and Support Services

Delivery of Seller systems and hardware/software components by default include 12 months (1 year) of Systems Software Maintenance and Support Services.

Subscription to Systems Software Maintenance and Support Services includes access to Seller tools and driver software compatible with future releases of MathWorks software and professional technical support by phone and e-mail.

Subscription to Systems Software Maintenance and Support Services does not include free updates of existing custom implementations (FPGA bitstreams).

Software Maintenance and Support Renewal

For uninterrupted Systems Software Maintenance and Support Services in subsequent years Buyer may opt to renew its subscription annually to maintain its investment. Reinstatement if elapsed is possible on request, but incurs back maintenance charges of up to 6 months. Staying subscribed is the most cost-effective way to access latest advances and technical support.

7.4 Use of Speedgoat Software Including Tools and Drivers

LEGAL INFORMATION ABOUT THE USE OF SPEEDGOAT TOOLS AND DRIVERS:

Speedgoat tools and drivers are optimized for hardware purchased from Seller and may be used only in conjunction with the hardware (serial No.) for which the tools and drivers were purchased for. Access to the Speedgoat tools and drivers is only available if the target machine component has active subscription to Systems Software Maintenance and Support Services.

Terms and Conditions for software components are defined in the Speedgoat End-User License Agreement (EULA).

8 Contact Information

For further information:

Sales	sales@speedgoat.com	
Support	support@speedgoat.com	
Call	Switzerland	+41 26 670 7550
	USA	+1 508 233 2650
	Germany	+49 5139 97780 50

Or log in to the Speedgoat Customer Portal: www.speedgoat.com/login